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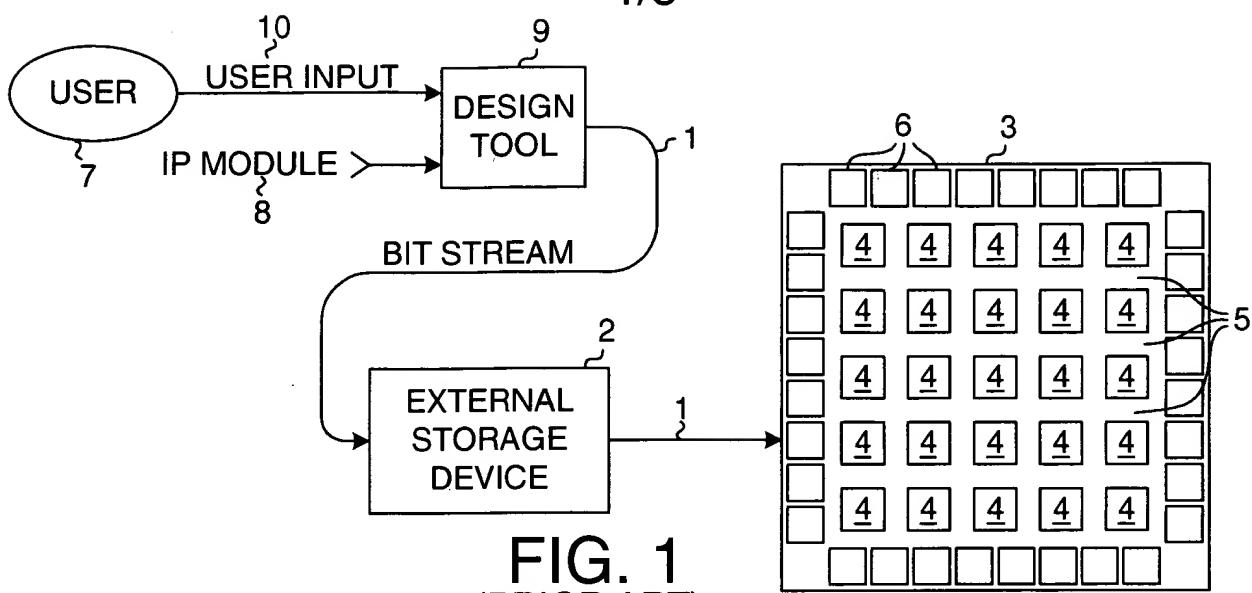
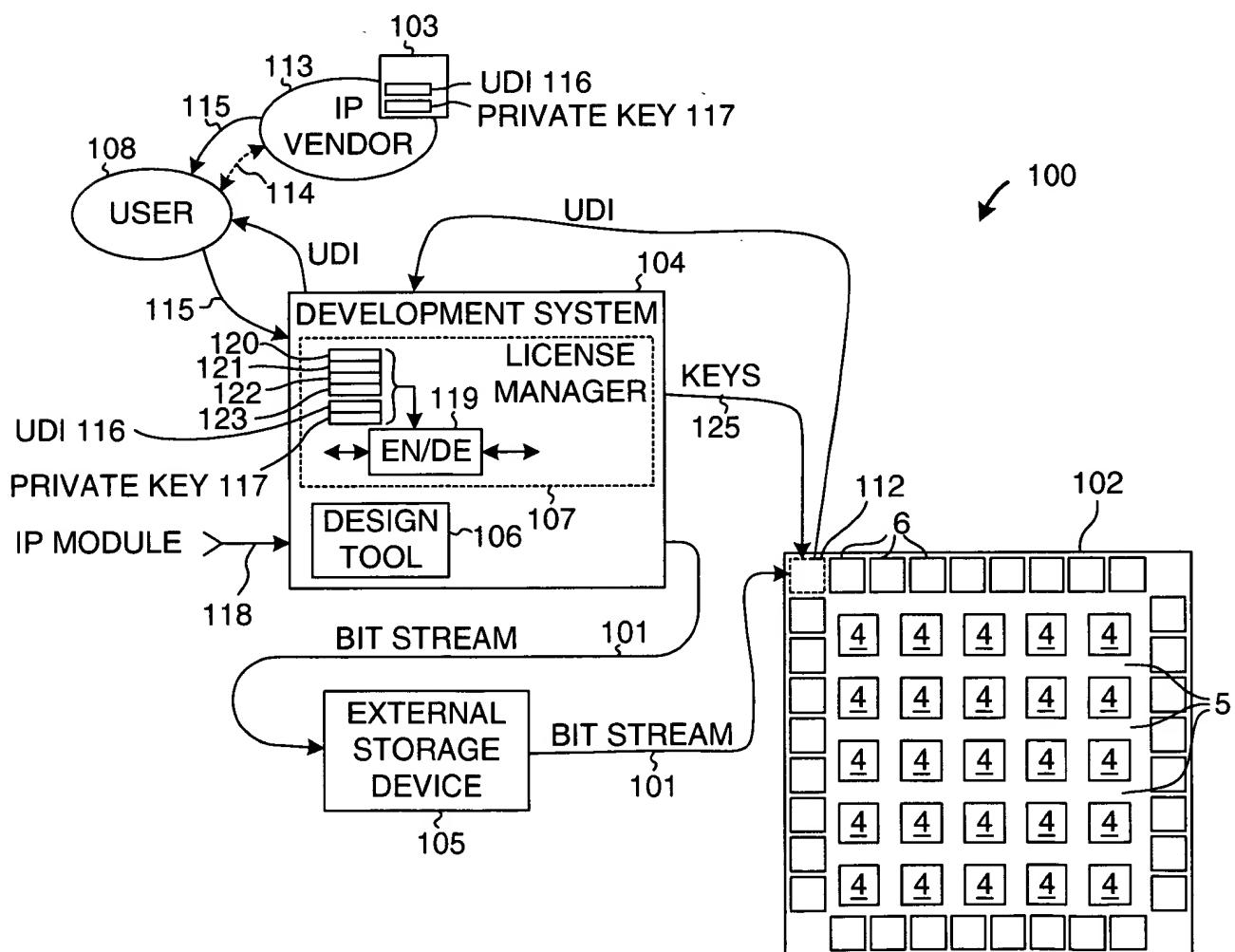
FIG. 1  
(PRIOR ART)

FIG. 2

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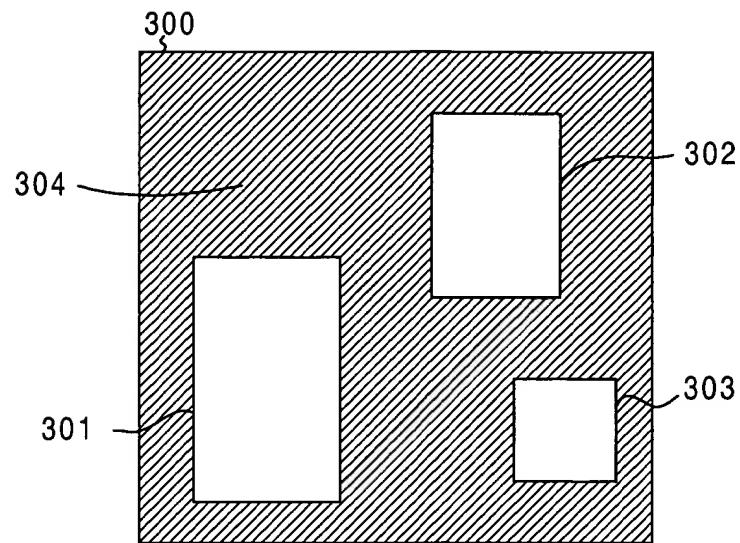


FIG. 3

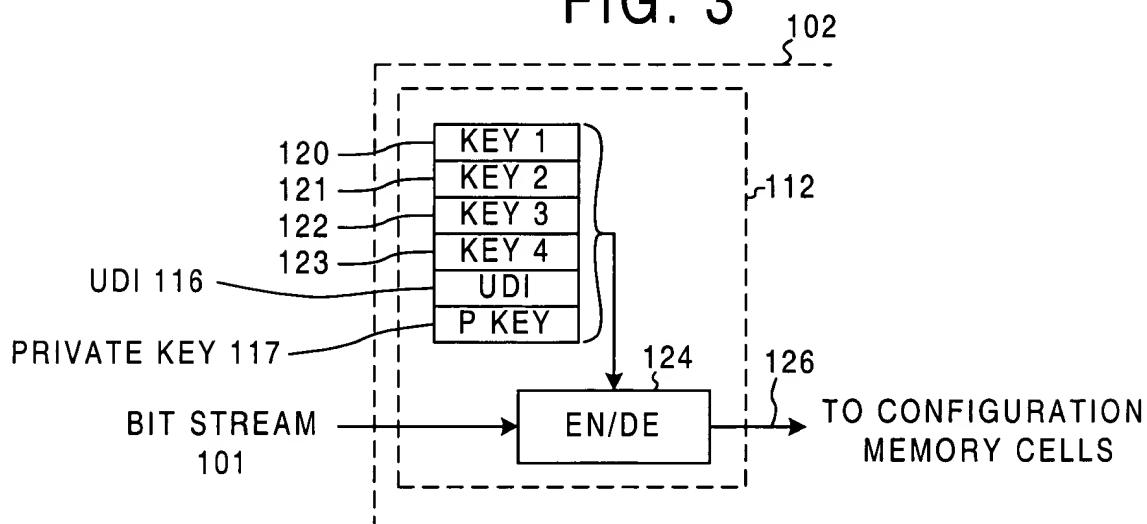


FIG. 5

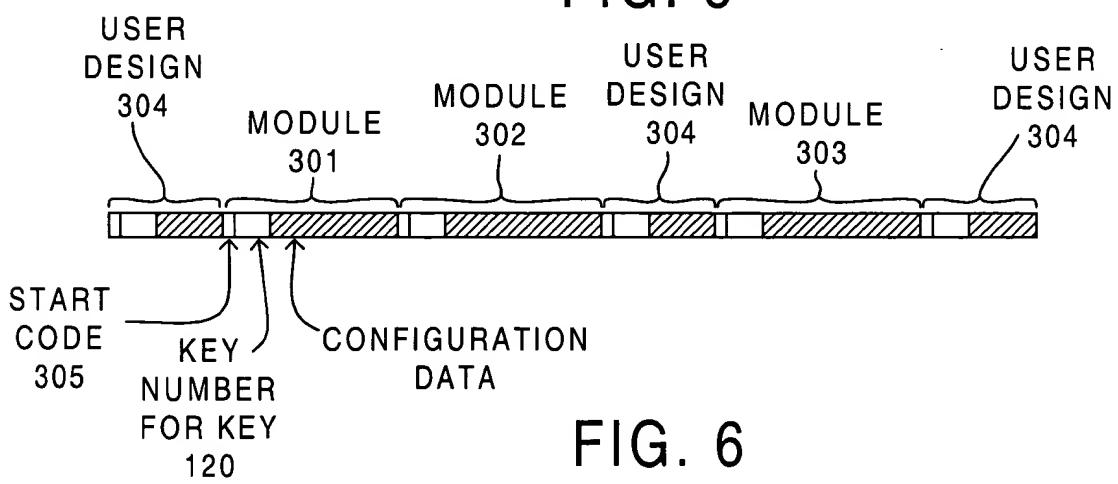


FIG. 6

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START

IP VENDOR SENDS AUTHORIZATION CODE TO A USER TO USE A PARTICULAR DEVELOPMENT SYSTEM TO IMPLEMENT A PARTICULAR IP MODULE ON AN FPGA THAT HAS A PARTICULAR UDI

LICENSE MANAGER QUERIES USER FOR AUTHORIZATION CODE

USER SUPPLIES AUTHORIZATION CODE TO LICENSE MANAGER

LICENSE MANAGER READS UDI FROM FPGA AND SERIAL NUMBER FROM DEVELOPMENT SYSTEM

LICENSE MANAGER VERIFIES THAT AUTHORIZATION CODE GRANTS ACCESS TO THE IP MODULE BY: 1) CHECKING THAT THE UDI READ FROM THE FPGA MATCHES THE UDI FROM THE AUTHORIZATION CODE; 2) CHECKING THAT THE SERIAL NUMBER OF THE USER'S DEVELOPMENT SYSTEM MATCHES THE SERIAL NUMBER FROM THE AUTHORIZATION CODE; AND 3) CHECKING THAT THE USAGE CONDITION IN THE UDI IS MET

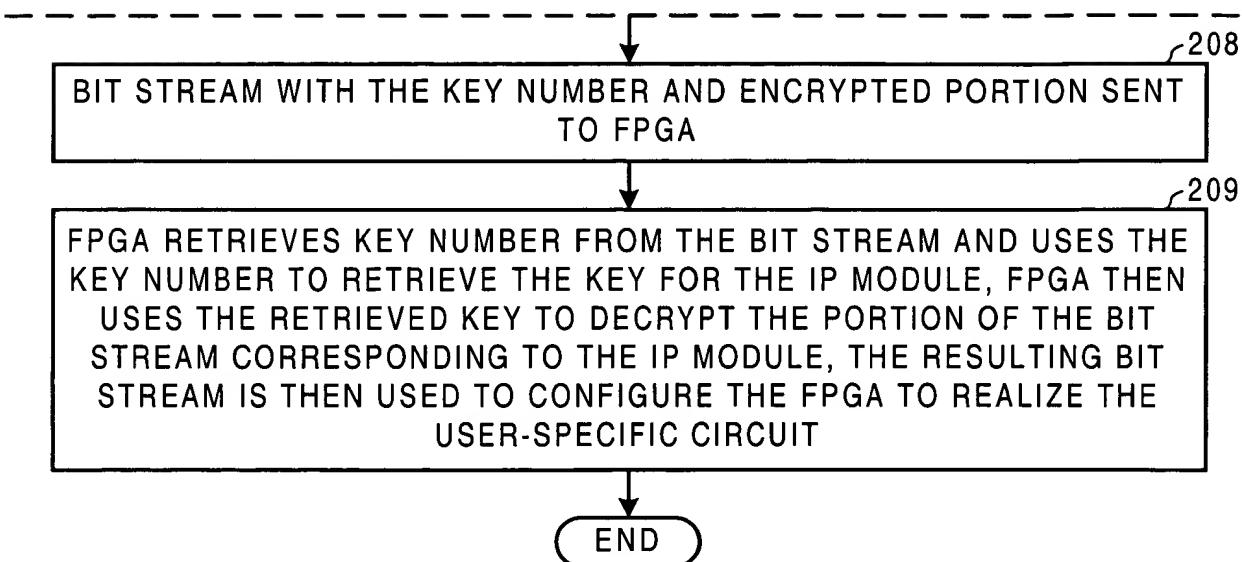
IF THE VERIFICATION IS MADE, THEN THE LICENSE MANAGER: 1) ALLOWS THE USER'S DEVELOPMENT SYSTEM TO ACCESS TO THE IP MODULE; AND 2) ENCRYPTS A KEY FOR THE IP MODULE USING THE UDI AND A PRIVATE KEY, AND SENDS THE ENCRYPTED KEY AND KEY NUMBER TO THE FPGA

FPGA USES ITS UDI ALONG WITH THE PRIVATE KEY TO DECRYPT THE ENCRYPTED KEY AND KEY NUMBER, FPGA STORES THE KEY IN ASSOCIATION WITH THE KEY NUMBER

WHEN USER HAS DESIGNED USER-SPECIFIC CIRCUIT EMPLOYING THE IP MODULE, THE DESIGN TOOL OUTPUTS A BIT STREAM FOR THE USER-SPECIFIC DESIGN, BEFORE THE PORTION OF THE BIT STREAM CORRESPONDING TO THE IP MODULE THE LICENSE MANAGER INSERTS THE KEY NUMBER FOR THE IP MODULE KEY, THE LICENSE MANAGER ENCRYPTS THE PORTION OF THE BIT STREAM CORRESPONDING TO THE IP MODULE USING THE KEY

FIG. 4A

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KEY TO FIG. 4

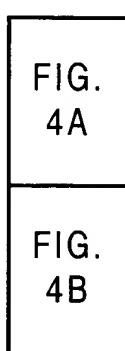


FIG. 4B

FIG. 4

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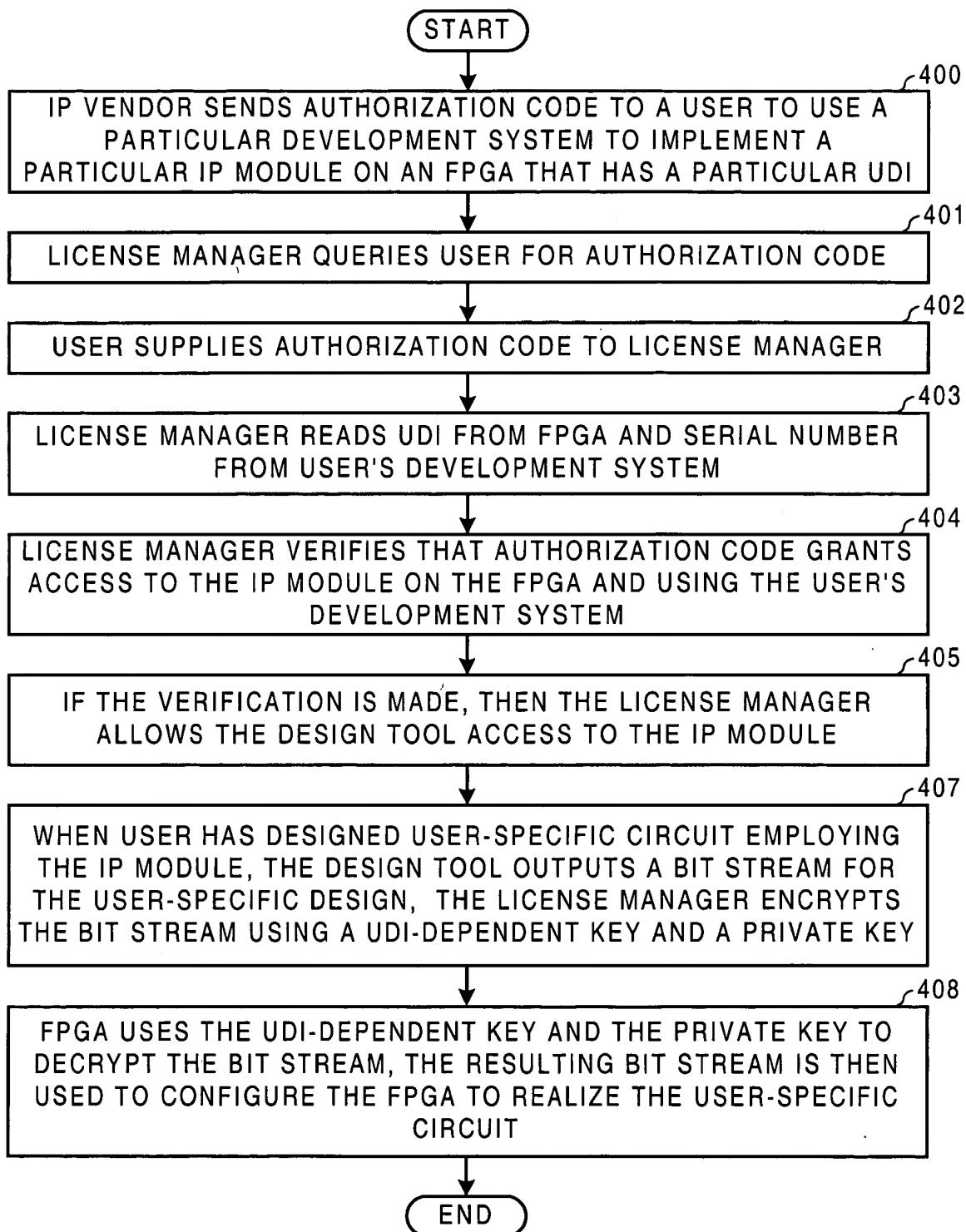


FIG. 7